R09

Code No: C6106, C0608, C7702, C6802, C5702, C6506

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech I Semester Examinations March/April-2011

CPLD & FPGA ARCHITECTURES AND APPLICATIONS

(COMMON TO COMMUNICATION SYSTEMS, DIGITAL SYSTEMS & COMPUTER ELECTRONICS, EMBEDDED SYSTEMS & VLSI DESIGN, VLSI&EMBEDDED SYSTEMS, VLSI SYSTEM DESIGN, WIRELESS & MOBILE COMMUNICATIONS)

Time: 3hours **Max.Marks:60**

Answer any five questions

All questions carry equal marks

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1. a. Explain the design of altera flex logic -1000 series cpld.
   b. Explain The Pla Design With An Example. [12]

2. Explain Cypres Flash 370 Device Technology. [12]

3. a. Explain the fpga with channel and channel less gate array. Explain routing technique implemented.
   b. Explain the design aspects of altera's flex 8000 fpga. [12]

4. Explain the microprograming linked state machine with an example. [12]

5. a. Explain the properties of petrinets.
   b. Explain the state machine for petrinets with an example. [12]

6. Explain the design flow using fpga mentor graphics eda tool. [12]

7. Design a parallel adder sequential circuit. [12]

8. Write short notes on the following.
   i. Speed performance of actel.
   ii. Speed performance in system programmability.
   iii. Asic design flow. [12]

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